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RE:	Our Docket No.: 50M2895.02 (1168-99.CON) U.S. Serial No.: 10/656,031	

Transmitted herewith are pages 2-5 of the above-refgerenced application.

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compression algorithms and produces as an output a video bitstream requiring substantially less transmission bandwidth that would have been required for the original video signal information. After transmission of that compressed video bitstream to a receiving site, that bitstream is operated on by a decoder which reverses the compression process and restores the original video signal information.

A widely-accepted standard for the encoding and transport of such digitized video signal information is the MPEG-2 Standard, the details of which are set forth in the International Organisation for Standardisation's International Standard Document ISO/IEC 13818-1, *Information Technology -- Generic Coding of Moving Pictures and Associated Audio Information: Systems* (November 1994), which Standard Document is incorporated by reference herein. The discussion herein is based on the application MPEG-2 encoded video signals and MPEG-2 compliant decoders, but it should be understood that the invention described herein is not limited to a particular encoding/decoding method or standard.

Digital video decoders such as found in digital television receivers or in set- top boxes (STB), require accurate synchronization between the encoding rate of the incoming video signals -- *i.e.*, the rate at which an input video bitstream is encoded by at a transmission site, and the decoding rate of such signals -- *i.e.*, the rate at which the input video bit-stream is decoded by the digital video decoder receiving the encoded video bitstream. Because the received data is expected to be processed at a particular rate -- to match the rate at which it is generated and

transmitted, a loss of synchronization between the decoder and the encoder leads to either buffer overflow or underflow at the decoder, and as a consequence, loss of presentation and/or display synchronization.

Generally, synchronization in such video decoders occurs in a two-stage process. In the first stage, a digital video decoder analyzes the incoming video bit stream transmitted by the encoder to determine the clock frequency, or base clock, of the encoder. A standard method of clock-recovery at the decoder with respect to MPEG-2 digital video signals is described below in the Detailed Description. In the second stage of synchronization, the decoder uses the recovered base clock rate of the encoder to reproduce video frames at exactly the same rate as that of the transmitter's encoder. This decoder processing includes an extraction of fields from the video bitstream containing decoding and presentation time stamps as well as various video format attributes. For an MPEG-2 compressed video signal, such attributes include the number of pixels per line, the number of lines per frame, and the number of frames per second. These attributes, and thus the respective video formats, differ for standard definition (SD) video and high definition (HD) video.

In particular, it is noted that the "normal" frame rates for the HD and SD video formats are respectively 30 Hz and 29.94 Hz. Note also that 29.94 Hz is the frame rate for the analog NTSC video system and that the SD video format supports corresponding pixels/line and lines/frame rates to those of the NTSC system. Thus, the 29.94 Hz frame rate may be viewed as being somewhat of an artifact from the analog NTSC video system.

A synchronization issue for the decoder is, however, presented by these different frame rates because the MPEG-2 standard permits the application of either frame rate to either the HD or SD video format -- reflecting both an expectation that some NTSC-produced program material will be transmitted using the HD video format, and the possibility that, in the long run, the SD video format may utilize primarily the 30 Hz

frame rate. However, for the indefinite period during which both HD and SD formatted programming is transmitted at both the 30 Hz and the 29.94 Hz frame rates, a necessity exists for the decoder to adapt to the "non-standard" frame rate for a video bitstream in which it occurs. For example, a decoder processing an HD bitstream which was encoded and transmitted using the 29.94 Hz frame rate will experience input buffer underflow and loss of presentation and/or display synchronization unless such an adaptation is made from the expected 30 Hz frame rate for that format. In the alternate case of processing an SD bitstream encoded and transmitted at a 30 Hz frame rate, input buffer overflow would be experienced, along with similar loss of presentation and/or display synchronization.

SUMMARY OF THE INVENTION

Accordingly, it is an object of the invention to provide a mechanism to achieve decoder synchronism in the circumstance of the encoded frame rate being other than the frame rate expectation of the decoder for the video format being processed. To that end, a method of employing an adaptive clocking mechanism to modify the frame rate of a decoding system of a digital display system is disclosed which includes the following steps. In one step, format information, including the encoded frame rate, is derived from a video bit-stream received by the digital display device. In another step, a modifier is selected based on the format information derived from the video bit-stream. Finally, the frame rate is modified by applying the selected modifier to a member of the group consisting of a system time clock and a system clock frequency.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of a known clock recovery system in a digital video decoder.

FIG. 2 is a block diagram showing an embodiment of the adaptive clocking mechanism of the invention.

FIG. 3 is a block diagram showing another embodiment of the adaptive clocking mechanism of the invention.

DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT

Exemplary embodiments of the timing synchronization mechanism of the invention will now be described in detail with reference to the accompanying drawings. It will be appreciated by one skilled in the art that the inventive concepts disclosed and discussed in detail with reference to the exemplary embodiments herein can be employed to synchronize the frame rate of a digital video decoder which is either integrated within a digital display device -- *e.g.*, an integrated digital television receiver/decoder, or which is in a device which is in communication with (although not necessarily physically connected to) a display device -- *e.g.*, a digital set-top box (STB). It will also be understood that the inventive concepts herein are intended to apply to environments where, for example, either or both the clock recovery process and the bitstream decoding process may occur within the digital display device itself (*e.g.*, within an integrated digital television receiver/decoder), or in a digital STB or other similar digital decoding device. For simplicity of illustration, the inventive concepts herein are discussed with reference to a digital video decoding device that includes both the system clock recovery mechanism and decoding mechanism.